Development of 128M DRAM by Stacked Packaging Technology

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Abstract

Demand for the larger memory capacity within smaller space in the high-end computer system has created the need for highly integrated chips. However, since the ICs such as 256MDRAM is not available yet in a large quantity, Samsung's proprietary package technology was developed to fulfill the demand. In this project, two 64MDRAMs were integrated to 128MDRAM by stacking technology. The lead frame design for the top and bottom packages were the same, and the different bonding option distinguished the top part from the bottom part. Through the development, all potential problems in mass production were cleared, and the assembly quality and the package reliability were accomplished to be within the international specification.

I. INTRODUCTION

1. Background

The demand of memory usage for the high-end system tend to increase 8 times every 3 year. But the density of memory device has increased to 4 times by the same terms. In order to solve the problem which is emerged by the memory density difference between provider and user, system

manufacturers have used memory in the form of module. For example, the memory module 2Mx36 is made by mounting 1M memory devices on the both sides of PCB (Printed Circuit Board) and 8Mx36 is made by using 4M memory devices. The size of PCB is restricted by the trends of the system which tends to be lighter, thinner, shorter, and smaller in size. The multimedia technology drives the performance of PC (Personal Computer) to be equal to that of high performance work station. Therefore, PC requires the better memory specification such as larger size, minimal signal delay, and fast signal processing speed. Many semiconductor makers have to seek new advanced fabrication technology and also new packaging technology to fulfill customer's requirement. In order to increase memory density, they prefer to develop packaging technology to the fabrication technology which requires much more financial investment and developing time.

DRAM Stacked Package is developed to provide a transitional solution for the above problems. The stacked package can achieve the following enhancements; minimizing the mounting area of device, increasing the memory density, and reducing the propagation delay due to the simple PCB design.

In order to overcome the above limitations, there needs 128MB DRAM by stacking two 64MB DRAM devices. Samsung Semiconductor has developed a 128MB stacked package by using two 32 pin packages of 64MB DRAM. It also provides a solution to expand memory density that can be mounted on the existing PCB without modifying design. Figureure1 shows different memory density and time of development of between Stacked package and one chip package

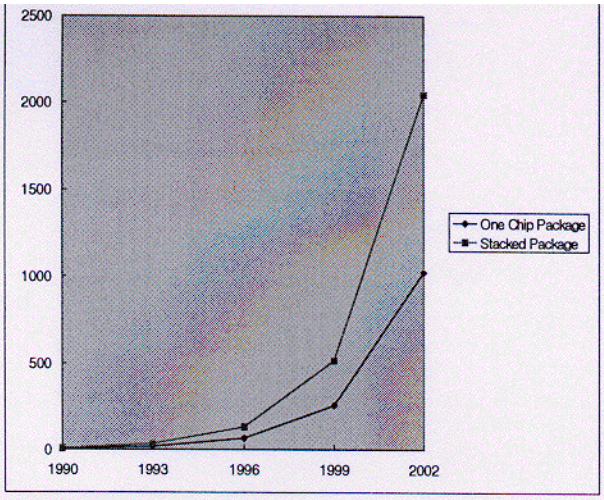


Figure1: Comparison Stacked package to one chip package

2. Making A Stacked Package

2.1 Pin Configuration

Figure.2 and Figure.3 shows two different options of 64MB DRAM pin configurations. The first example is made by splitting data pins and the 2nd example is composed of splitting /RAS signal to make 2 banks. End-users can choose a proper type from options for their requirements. The 4 different pin configurations of above packages are made from a common leadframe by using different wire bonding options. Since, those top packages from Figure.2 and Figure.3 have the same pin configuration as the existing 32 TSOPII 64MB DRAM does, they can be used as a single component.

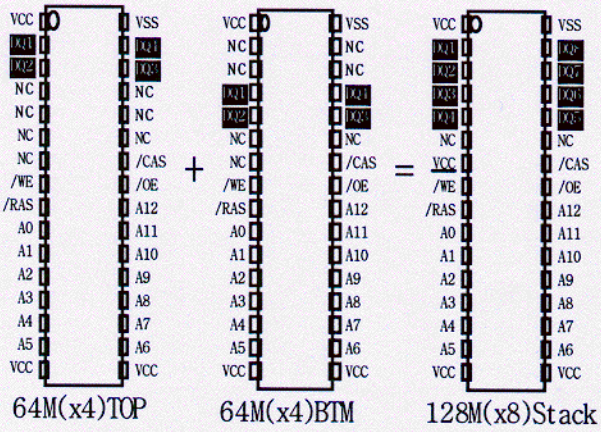


Figure 2 : Pin Configuration of 16Mx8 (Two 16Mx4)

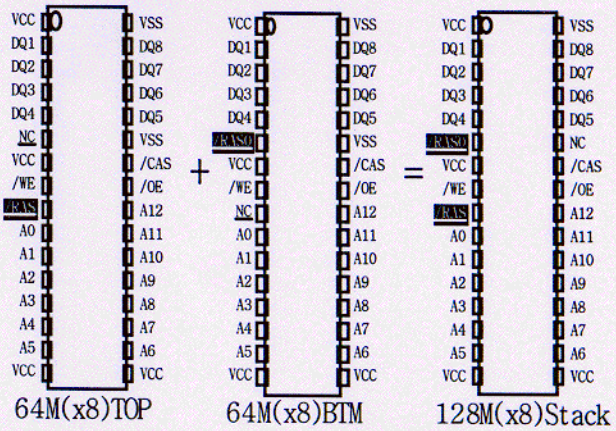


Figure 3 : Pin configuration of 16Mx8 (Two 8Mx8)

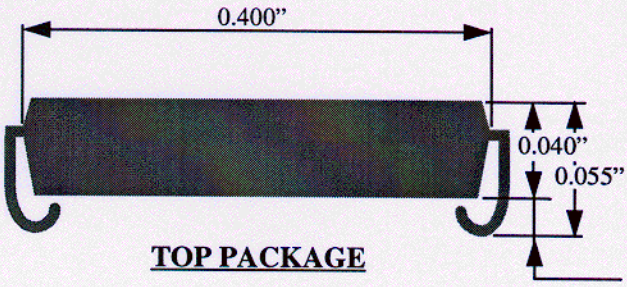
2.2 Bonding Options

Figure.2 shows bonding diagrams of top and bottom packages to make a 128MB (16Mx8) stacked DRAM by using different bonding options on the same leadframe. Pin #2, #3, #30, and #31 of top package are connected to data I/O of chip and pin #4, #5, #28, and #29 are assigned as NC (No Connection). But the data pins and NC pins of bottom package are switched their connections to the chip. Data I/Os are splited their assignment on top and bottom package and all the other pins are assigned with the same Configurations. Since there is no conflict in data I/O assignment on top and bottom chips, both 64MB DRAM chips are operating together in a signal clock as if it is 128MB (16Mx8) DRAM chip. Figure.3 describes another way of bonding options to make a 128MB DRAM (16Mx8) by stacking two 64MB DRAMs (8Mx8). The bonding options of /RAS pins enable to increase memory density but also enable to work them in 2 banks by providing chip selecting function. The pin assignments of the top package are configured as those of the existing 64MB(8Mx8 EDO) DRAM. Pin #10 is assigned as /RAS and pin #7 is left as the only NC on the bottom package. On the contrary, pin #7 is connected to /RAS0 and pin #10 is left as NC on the top package. All the other pins are assigned with the same configuration on both

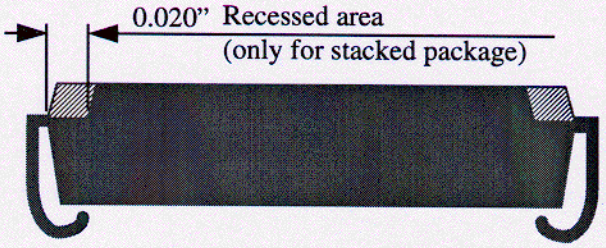
packages. This configuration enable to work both 64MB DRAM chips without data conflict as if 128MB (16Mx8) DRAM works in 2 banks, when they are processed by a /RAS signal.

2.3 Package Structure

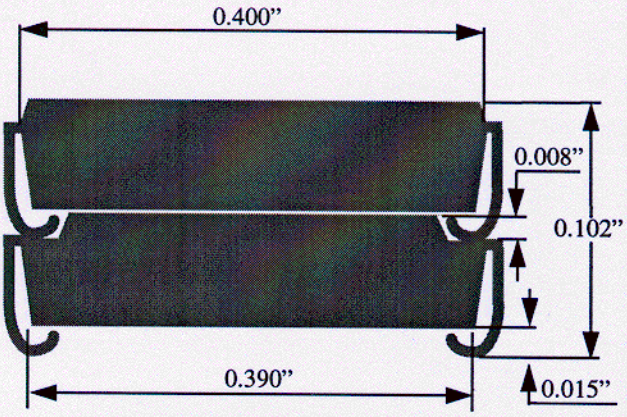
The total height of Samsung's stacked package which uses two 32 TSOJ packages is higher around 2 times than that of TSOPII type and around 2/3 of the total height of SOJ. However, the area which needs to mount the above packages are all same. In other words, the memory density can be increased to 200%.



TOP PACKAGE



BOTTOM PACKAGE



STACKED PACKAGE

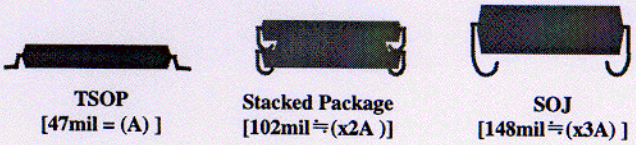


Figure 4: The structure of Stacked Package

The following sections will describe the difficulties and solutions of the stacked packaging process. The problems and solutions of molding process, especially, for the new package type TSOJ are described. The process conditions for stacking such as tin plating and coplanarity are also explained. The results of electrical test and reliability test after finishing assembly are represented finally.

II. Stacking Package Assembly

1. Process Flow

Table 1 shows the assembly process of stacked DRAM package. As seen in Figure. 4, a unit package is assembled in existing process without adding new assembly process. The stacking process is the only additional process to make stacked package.

Process Flow	Condition
D/A ↓ W/B ↓ Mold ↓ Post Cure ↓ Trim ↓ Tin Plating ↓ From ↓ Test ↓ Burn-In ↓ Stack ↓ Test → Packing ↓ Module Ass`y ↓ Test ↓ Packing	*All the same process condition of Samsung TSOP Package Ass`y Process.(Except Stack & Stack Test) *The Stack Test is only Open Short

Table 1, Process flow chart

2. Results of Process Evaluation

The major difference of the stacked packaging process from the existing packaging process is to make a 3-D package by stacking 2 different outline shapes of package. The pin configurations of top and bottom packages are different as described before.

2.1 Wire Bonding

Loop height is measured at the point of the top of pin #6(/RAS) as in Figure.5. Bonding wire passes about 40~70 ㎛ over the bus bar. It is possible to control the height of loop height as stable and low as 225 ㎛~276 ㎛ by applying the optimized lead frame design.

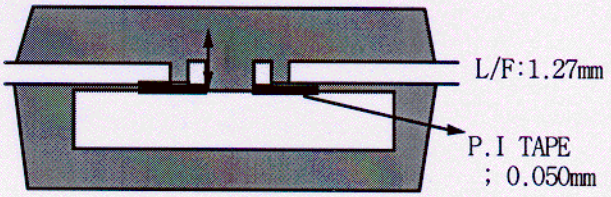


Figure 5: Wire loop check

2.2 Molding

While molding was processing, wire sweeping, chip cracking, and die shifting were examined every 10 shots up to total 60 shots, and they were checked every 20 shots after total 60 shots but before total 180 shots. Chip cracked sample was not found at all after decapsulation. There was chip shift phenomenon within 1 mil. The amount of wire sweeping is ranged 5 ~ 10% after taking X-ray measurement. The shape of the warpage of package was concaved top side and the amounts of warpage which ranged from 10 ㎛ to 25 ㎛. (See **Figure 7**)

.3 Plating and Chemical Deflash

Plating is a critical factor to make stacked package. The reason why the current density was not raised over 90A was to prevent from occurring bad plating quality such as rough surface. In order to get stable and dense structure of solder, only the moving speed was controlled. The difference between 2nd and 3rd measurement in Table 2 may be due to the difference of the number of sample.

No	Condition	Result	Remark
1st (10 Strip)	- 90A - 3.0m /min	- Avg.;22.04 - Max.;24.26 - Min.;19.01	- Normal Condition * Current = 65A * Time = 4.2m/min
2nd (10 Strip)	- 90A - 2.5m /min	- Avg.;23.89 - Max.;26.93 - Min.;22.36	
3rd (30 Strip)	- 90A - 2.0m /min	- Avg.;23.59 - Max.;26.79 - Min.;20.47	
Mass (800 Strip)	- 90A - 2.5m /min	- Avg.;19.50 - Max.;21.67 - Min.;17.63	

Table 2 : Tin plating conditions

When the condition of 2nd sample was applied to the mass sample case, thickness of tin plating was measured 4 ㎛ less than that of 2nd sample. The reason was that the current density got increased as the number of sample got reduced. The amount of resin bleed on bottom of package was about 20 mils over the exposed lead frame along the package outline (Table 3, Figure. 6). The process of chemical deflashing for the tin plating is also effective to deflash the resin bleed. Though the around 5mil of non-plated area was found on the both lead frame side of package as in Figure. 6, there was no problems in stacking process because the point which was landed from top package to bottom package was 15 mil outside from the body.

Sample	Value(mm)	Sample	Value(mm)	Sample	Value(mm)	Sample	Value(mm)
1	0.45	6	0.47	11	0.48	16	0.53
2	0.51	7	0.49	12	0.52	17	0.52
3	0.50	8	0.51	13	0.48	18	0.54
4	0.52	9	0.48	14	0.52	19	0.48
5	0.51	10	0.52	15	0.49	20	0.51

Table 3: Measurement of mold resin bleed

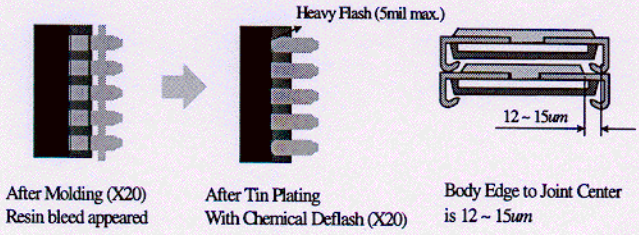


Figure 6 : Resin bleed appeared area

2.4 Form

After forming process, measurements of critical points such as package width, length, recess width, thickness, and stand-off are all within the specification. The most controversial point of coplanarity was measured from 33 ㎛ to 65 ㎛. The principal reason for the unstable coplanarity was assumed to be warpage of package. The changes of plating thickness from 10 ㎛ to 20 ㎛ and unstable form process were also considered to provide reasons for producing unstable coplanarity. Considering the amount of warpage was ranged from 10 ㎛ to 25 ㎛ and coplanarity was ranged from 40 ㎛ to 70 ㎛, the tolerance which was produced from the forming process was assumed to be around 50 ㎛ .

(see **Figure 7**).

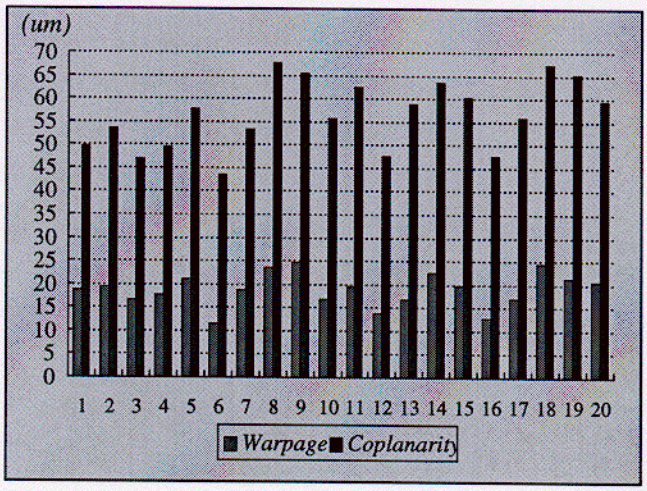


Figure 7: Warpage Vs Coplanarity

3. Stack Process

Figure.8 shows how the stacking process is operated. The bottom package is picked from unloader tray and placed to the stack jig. Then the top package is placed on the top of bottom package after applying flux on leads. The top and bottom packages which are hold in the stack jig pass through hot air zone to solder.

3.1Assembly Tin + Flux Only

3.1.1 Conditions of stacking Test

In order to evaluate solder joint reliability of each stacked package, the thickness of tin plating, coplanarity, and the direction of warpage are considered in 5 different way as shown in Table 4.

※ D: Concave shape warpage

N: Convex shape warpage

No.	Warpage	Plating	Coplanarity	Quatity
1	N	2.5m/min.	2mil	16
2	N	2.5m/min.	3mil	16
3	N	2.0m/min.	3mil	16
4	D	2.5m/min.	2mil	16
5	D	2.5m/min.	3mil	16

Table 4, Stacking test item

3.1.2 Stacking Evaluation

.Solder joint reliability was evaluated by inspecting all of solder joints visually using X20 low scope. The shape of solder fillet was distinguished into 3 different groups as follows:

F = Full Fillet (normal fillets on 3 faces: front and 2 sides)

R = Recessed Fillet (small fillet on front face and 2 normal side fillets)

S = Side Fillet (very weak fillet on front face and 2 normal side fillets)

No	Number of R	Number of S	Number of F	Remark
1	23	17	472	R+S=40
2	34	8	470	R+S=42
3	6	-	506	R+S=6
4	14	19	479	R+S=33
5	31	30	451	R+S=61

Table 5 : Stacking test result.

Visual inspection on the number of 2560 solder joints resulted that all of them were in good fillet shape, though there were a little deviations in number and shape of solder fillet.

The effects of coplanarity and warpage on solder joint reliability were not revealed well in visual inspection.

Though more F shape fillet were found in the group of 2mil coplanarity sample than in the group of 3mil coplanarity sample, the absolute number of different were not so big nor the direction of warpage had a tendency.

The most effective factor was the thickness of tin plating. The number 3 condition which made thicker tin plating by slowing down the belt speed in plating process produced the highest outcome of full fillet. 506 solder joints out of 512 joints was formed in F shape solder fillet which was equal to 98.8% of total samples. Placement tolerance of X-axis mismatch was higher than that of Y-axis mismatch. The maximum amount of mismatch was 3.6mil in X-axis and 2.7mil in Y-axis. The tendency of placement tolerance was not clearly shown to be related with experiment conditions.

3.2 Solder paste evaluation

In order to enhance the reliability of solder joint by providing additional solder, solder paste is applied at stack solder joint. Various solder paste are applied by adjusting the amount of flux to change the viscosity of solder paste. The soldering process has been tried in various temperatures which are controlled by the amount of hot air.

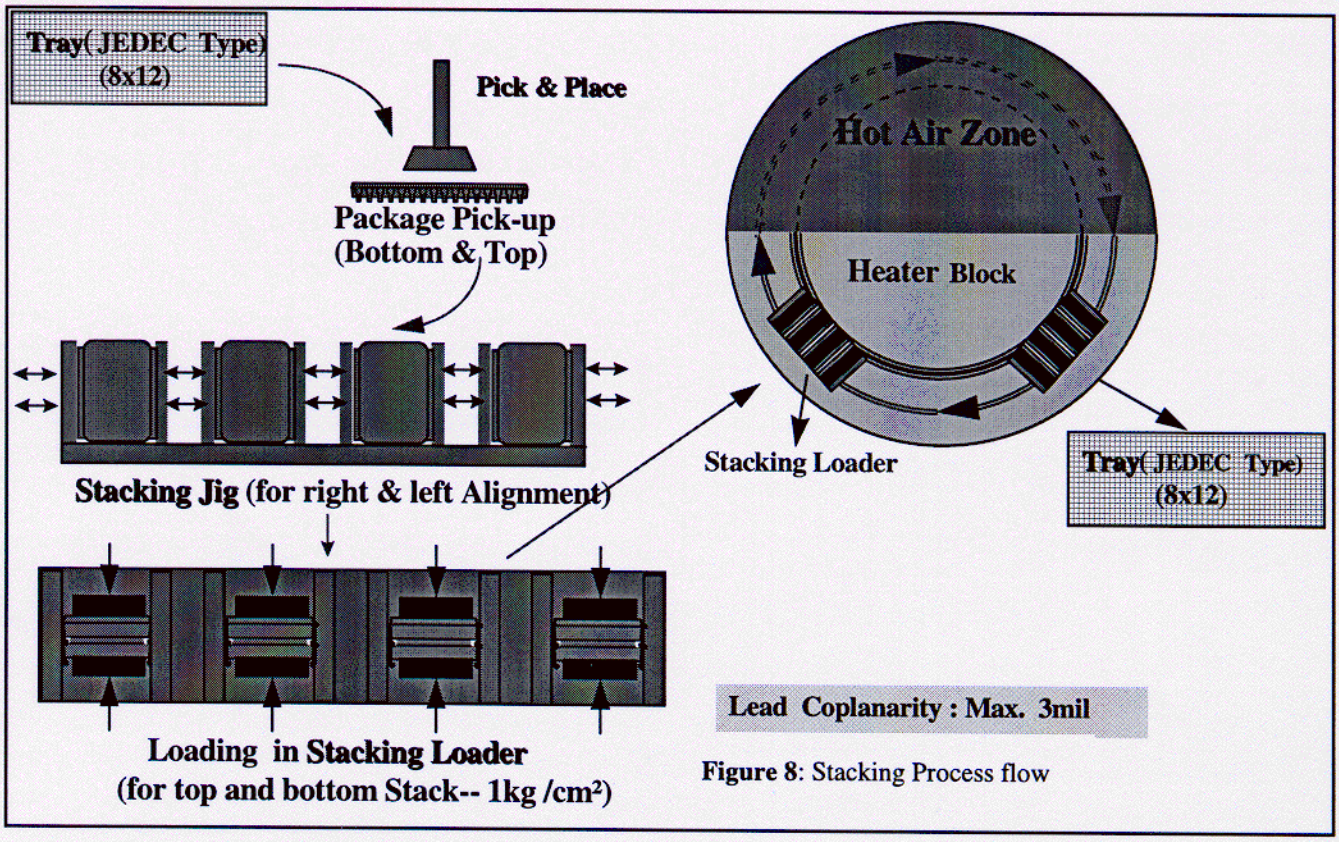
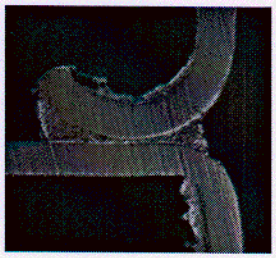


Figure 8: Stacking Process flow

Applying solder paste on lead frame is processed by touching on the rubber roller which travels through the container of solder paste. The amount of solder paste on the rubber roller is controlled by the Teflon or metal guide. The temperature of hot air was set in 3 different ways of 360 ℃, 380 ℃, and 400 ℃. The result of applying solder paste was better surface condition and solder joint shape than in case of applying only flux. There was problem in the uniformity of solder paste on lead frame which affected the shape of fillet on solder joint. The problem was resolved by changing the material of roller and adding metal guide to control the height of solder paste.

9-A: Coplanarity



9-B: Tin Plating only

9-C : Solder paste

Figure 9 : Solder joint view

4. Comparison of lead pull strength

Figure. 10 shows the test method of lead pull strength Test.

Measurement result:

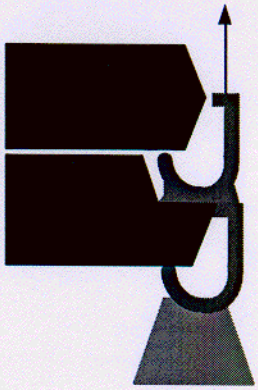


Figure 10; Method of solder joint pull strength

*Flux Only Type: 250g ~ 1115g / pin

*Solder Paste Type: 700g ~ 1950g / pin

The assembly process with solder paste provides much better mechanical characteristics than another process, when pull strength tests are performed under the same condition.

5. Electrical Test, Reliability and Thermal Characteristics.

5.1 The Result of Electrical Test Sorting

1st test ; Unit & Stacked Package

Device		Room Temp Sort	Hot Sort (Burn-In)	Stack	Remarks
16Mx4	Top	674/690	627/672	602/612 (98.26%)	- Fail parts are almost O/S Fail (Misalign/Bent Lead/Jamming)
	Bottom	673/695	612/673		
	Yield	97.25%	92.11%		
8Mx8	Top	691/716	619/691	581/605 (96.33%)	- Rework & Retest 100% Good
	Bottom	697/716	620/697		
	Yield	96.93%	89.3%		

2nd test ; Stacked Package (For verification of stack)

Device		Room Temp Sort	Remarks
16Mx4	50ns	184/193 (95.34%)	- Fail parts are almost O/S Fail. (Excess Solder/Misalign / Jamming on hander)
	60ns	479/488 (98.35%)	

5.2 The Result of Reliability Test

◆ *Unit Package & Stacked Module Pre-condition Data*

Temp. / PKG..	85℃/65% (168hrs)	Temp. Cycle (65 ~ 155℃)	IR.. Reflow (235℃)	Remark
Top Package	0/116			
Bottom Package	0/116			
Stacked Package With PCB	0/10 Modules (Visual Inspection)			-32EA Stacked Package Mount

◆ *Unit Package Long Term Reliability Data*

- Soak: 85C / 65%, 1000Hrs
- Pressure Cooker Test (121 C , 2 atmosphere, 240 Hrs) ➡ *All passed*
- Temperure Cycle Test (-65 C~ 155 C / 1000 cycles)

◆ *Stacked Temperature Cycle Data*

Cycle / S/J		300cyc.	600cyc.	1000cyc.	Remark
Solder Joint (0 ~ 125°C)	Dummy stack	0/116	0/116	0/116	32TSOJ Stack

>> Double sided reflow soldering + Procondition <<

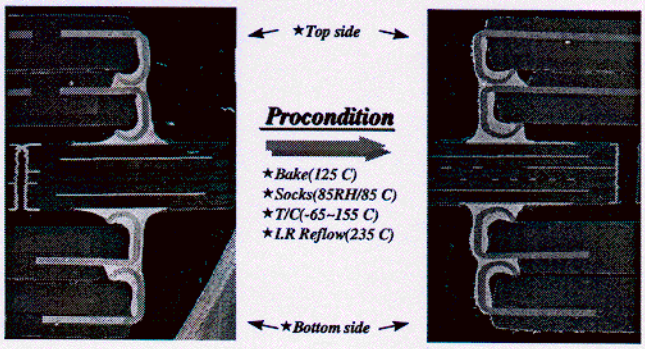


Figure 11: Solder joint of after SMD reflow soldering and precondition test

5.3 Measurement of Thermal Resistance

Tj of component package and stacked package were compared as shown in Figure 12. Tj of stacked package was 20% higher than that of component package when the operating power was 0.3W. The difference of Tj between component package and stacked package got bigger as the operating power increased.

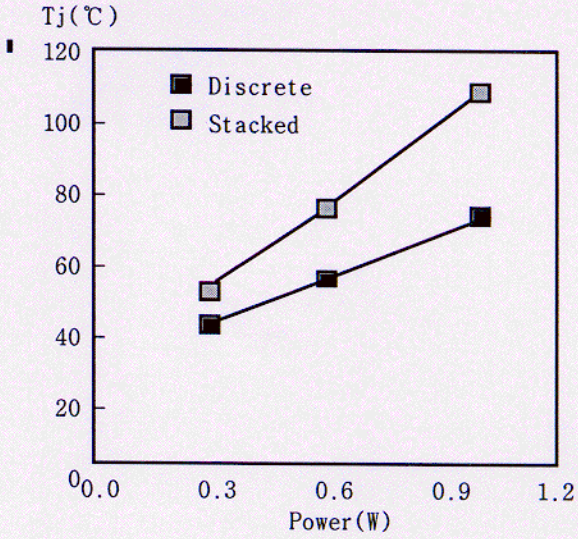


Figure 12: Thermal resistance measurement

III. Conclusion

A 128MDRAM which is made by stacking 2 64MDRAMs provides an example that the memory density can be doubled only by applying packaging technology. Because the existing process is applied, the mass productivity of stacked 128MDRAM is very stable and good. The electrical characteristics of stacked 28MDRAM is superior to the conventional memory module. The reliability of unit package is met with 85 ℃ /65% 168hrs condition. Temperature cycle test (-65 ℃ ~ 150 ℃) is being processed upto 1000 cycles. Stacked package also has passed temperature cycle test (0 ℃~ 125 ℃) upto 1000 cycles. Though there was a problem of resin bleeding on the bottom package, it was resolved after adding additional process of chemical deflashing. Though the developed stacking process can guarantee the good solder joint quality, is not easy to perform visual inspection. When flux is applied on solder joint, it resulted contamination problem and required cleaning process. To ensure solder joint reliability, additional solder paste is applied. Though the additional solder paste increase solder joint strength and resolve the contamination problem, it was very difficult to adjust temperature profile.

IV. References

1. R. J. Klein Wassink, "Soldering in Electronics 2nd Ed." Electrochemical Publication Limited, 1989.

2. Robert Crowley, "Three-Dimensional Electronics Packaging: A Multi-Client Study," TechSearch International, Inc., 1993.